PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Takumi HASEGAWA

Appln. No.: 09/273,560

Confirmation No.: 7269

Filed: March 22, 1999

For: DELAY ANALYSIS SYSTEM

Docket No: Q53743

Group Art Unit: 2123

Examiner: Kandasamy THANGAVELU

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. The USPTO is directed and authorized to charge the statutory fee of $540.00 and all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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Date: August 24, 2009

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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I. REAL PARTY IN INTEREST

The real party in interest is NEC CORPORATION by virtue of an assignment executed by Takumi Hasegawa on March 17, 1999, and recorded on March 22, 1999 at Reel 9844, Frame 0649.

II. RELATED APPEALS AND INTERFERENCES

To the best of the knowledge and belief of the Appellant, the Assignee, and the undersigned, there are no other interferences before the Board of Appeals and Interferences ("the Board") that will directly affect, or be affected by, the Board's decision in the present Appeal.

Applicants previously filed a Notice of Appeal on July 2, 2007 and subsequently filed an Appeal Brief on October 2, 2007. In response to the October 2nd Appeal Brief, prosecution was reopened as indicated in the Office Action mailed November 19, 2007.

III. STATUS OF CLAIMS

Claims 1-6 are all the claims pending in the application. Claims 1-6 have been rejected, and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

The Amendment Under 37 C.F.R. § 41.33, filed June 22, 2009, has been entered. (*See* Advisory Action dated July 22, 2009). Accordingly, there are no outstanding, non-entered amendments of the claims.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

A summary of the claimed subject matter follows in accordance with 37 C.F.R. § 41.37(v).

Claim 1

Claim 1 is directed to a delay analysis system, executed on a computer, for making a delay analysis of a logic circuit. Non-limiting embodiments of the delay analysis system are shown in FIGS. 1-6 and described generally at page 4, line 10 to page 9, line 9. The delay analysis system comprises

a delay analysis library comprising connection information and delay time information for a plurality of circuits (e.g., see FIG. 1(b), and Specification, page 5, line 20 to page 6, line 3); and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library (e.g., Specification, page 6, lines 4-18),

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information comprising delay time information for a signal path from input terminals to output terminals of a logical circuit of said at least one circuit, wherein the delay time information is specific to an input terminal logical state transition of the logical circuit and resulting logical state transition at an output terminal of the logical circuit, and wherein said delay time information for each signal path of the logical circuit of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to the logical operation information (e.g., FIG. 1(c), and Specification, page 6, line 19 to page 7, line 5),

wherein the delay analyzing module automatically analyzes the delay of the logical circuit based on the delay time information in said delay analysis library (e.g., FIG. 3 and Specification, page 7, line 6 to page 9, line 6).

Claim 2

Claim 2 is directed to a delay analysis system, executed on a computer, for making a delay analysis of a logic circuit. Non-limiting embodiments of the delay analysis system are shown in FIGS. 1-6 and described generally at page 4, line 10 to page 9, line 9. The delay analysis system comprises:

a delay analysis library comprising connection information and delay time information for a plurality of circuits (e.g., see FIG. 1(b), and Specification, page 5, line 20 to page 6, line 3); and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library (e.g., Specification, page 6, lines 4-18),

wherein, for each of said plurality of circuits, said library further comprises respective logical operation information comprising respective delay time information for a signal path from input terminals to output terminals of a respective logical circuit of each of said plurality of circuits, wherein the respective delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for the respective logical circuit of each of said plurality of circuits, and wherein said delay time information for each signal path of said plurality of circuits is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to the

respective logical operation information for each of said plurality of circuits (e.g., FIGS. 1(c), and 2, and Specification, page 6, line 19 to page 7, line 5),

wherein the delay analyzing module automatically analyzes the delay of the respective logical circuit of each of said plurality of circuits based on the respective delay time information in said delay analysis library (e.g., FIG. 3 and Specification, page 7, line 6 to page 9, line 6).

Claim 3

Claim 3 is directed to a computer-implemented method of making a delay analysis of a logic circuit. Non-limiting embodiments of the delay analysis system are shown in FIGS. 1-6 and described generally at page 4, line 10 to page 9, line 9. The computer-implemented method comprises:

referencing, using a computer, a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information for said plurality of the circuits, wherein the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, said delay time information for each signal path of said logical circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for said at least one circuit (e.g., see FIGS. 1(b) and 2, and Specification, page 5, line 20 to page 6, line 18); and

automatically selecting a delay time of each path of said logical circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information (e.g., FIGS. 1(c), 2, and 3, and Specification, page 6, line 19 to page 9, line 6).

Claim 4

Claim 4 is directed to a computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit. The computer-readable medium causes the computer to execute said method. The method comprises:

referencing a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information for said plurality of the circuits, wherein the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, said delay time information for each signal path of said logical circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by the logical

operation information for said at least one circuit (e.g., see FIGS. 1(b) and 2, and Specification, page 5, line 20 to page 6, line 18);

automatically selecting a delay time of each path of said logical circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information (e.g., FIGS. 1(c), 2, and 3, and Specification, page 6, line 19 to page 9, line 6); and

performing a delay calculation to determine a propagation delay time of the at least one circuit using said selected delay time of said logical circuit (e.g., Specification, page 8, line 16 to page 9, line 9).

Claim 5

Claim 5 is dependent from the delay analysis system set forth in claim 1. Claim 5 recites that the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed (e.g., FIGS. 3-6, and Specification, page 7, line 22 to page 8, line 6).

Claim 6

Claim 6 is dependent from the delay analysis system set forth in above-noted claim 5. Claim 6 recites that the logical circuit is an AND gate. When the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal. As such, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate. Consequently, the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case (e.g., FIG. 3, and Specification, page 7, line 6 to page 8, line 6).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following is a concise statement of each ground of rejection presented for review:

1. Whether claims 5 and 6 are properly rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement.

2. Whether claims 1-4 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,041,168 to Hasegawa ("Hasegawa '168") in view of U.S. Patent No. 5,528,511 to Hasegawa ("Hasegawa '511").

VII. ARGUMENT

Claim Rejections – 35 U.S.C. § 112

Claims 5 and 6 stand rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement. For *at least* the following reasons, Appellants respectfully traverse the rejection.

Appellants respectfully submit that claims 5 and 6 are supported by the Applicants' disclosure. For instance, the arguments submitted in the Amendment filed October 8, 2008 ("October 8th Amendment") sufficiently pointed out portions of the Specification and drawings which support the features recited in claims 5 and 6.

For example, claim 5 recites that the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed.

At least page 7, line 22 to page 8, line 6 of the Specification, and FIGS. 3-5 of the Appellants' drawings support the above-noted features of claim 5. FIG. 3 is a waveform diagram showing the rise and fall delay patterns of a 2-input AND circuit, according to a non-limiting, exemplary embodiment of the present invention. That is, FIG. 3 is an example of the claimed delay time information in the delay analysis library. In the case where the input 1 rises and the input 2 falls, the Specification discloses that "no terminal is selected for delay analysis" (Specification, page 8, lines 5 and 6). That is, when no change in a signal state of an output terminal of the logical circuit is determined (see FIG. 3, middle column – 'Rise/fall'), the delay

analyzing module determines that no further delay analysis needs to be performed. Moreover, this determination is necessarily automatic since it is based on the logical operation information of the logical circuit, which is stored in the delay analysis library. Therefore, Appellants respectfully submit that claim 5 complies with the requirements of 35 U.S.C. § 112.

Appellants further submit that the features of claim 6 are supported by the Appellants' disclosure. For example, claim 6 recites that the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case.

Appellants respectfully submit that the portions of the Specification and Appellants' drawings discussed above with respect to claim 5 also support the features of claim 6. It appears that the Examiner's position is that since the claim features at issue are allegedly not found explicitly in the Appellants' Specification, the subject claim limitations must not be supported by the Appellants' disclosure. **Appellants' respectfully submit, however, that there is no *in haec verba*—i.e., word for word—requirement for satisfying the written description requirement.** Therefore, contrary to the Examiner's assertions, Appellants are not burdened to

show where the claimed terms are explicitly recited in the Specification. **Rather, the newly added claim limitations can be supported in the Specification through express, implicit, or inherent disclosure** (*Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997 as cited in MPEP § 2163.02). Additionally, Appellants can show possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as **words, structures, figures, diagrams, and formulas** that fully set forth the claimed invention. *Id.*

Here, in a non-limiting, exemplary embodiment of the claimed delay time information shown in FIG. 3, it is shown in the middle column of the table in FIG. 3 (the 'Rise/fall' column) that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals. Further, it is shown that at a time at which the second clock signal among the two clock signals is input, the state is LOW which is the same state as the first signal state (i.e., at the first clock signal). Accordingly, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to the clock signal (see Specification, page 8, lines 5 and 6), and thus, in this case the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate. Therefore, the delay analyzing module, based on this delay time information, automatically determines that no further delay analysis needs to be performed as recited in claim 6. *Id.* As such, Appellants respectfully submit that claim 6 complies with the requirements of 35 U.S.C. § 112.

In response to the above arguments, the Examiner confusingly, and inaccurately, asserts in the Final Office Action mailed January 23, 2009 that the middle column of FIG. 3 ('Rise/fall')

is "totally incorrect" (Final Office Action, page 15, last paragraph, and page 17, first paragraph). Specifically, the Examiner thinks that the determination that no delay ('NONE') was caused by the input, as recited in claim 6, is incorrect. Appellants respectfully disagree.

For instance, as discussed in the Specification, and as pointed out during the phone interview conducted on April 16, 2009, since the state of the output is low both at the first clock signal (when input 1 rises), and at the second clock signal (when input 2 falls), it is determined that no delay was caused by the input (Specification, page 7, line 22 to page 8, line 6, and FIG. 3). As such, contrary to the Examiner's assertions, the determination of 'NONE" in FIG. 3 is justified.

In view of the foregoing, Appellants submit that claims 5 and 6 comply with the written description requirement.

Claim Rejections – 35 U.S.C. § 103

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,041,168 to Hasegawa ("Hasegawa '168") in view of U.S. Patent No. 5,528,511 to Hasegawa ("Hasegawa '511"). For *at least* the following reasons, Appellants respectfully traverse the rejection.

Appellants submit that even if the teachings of Hasegawa '168 and Hasegawa '511 are combined, they do not teach delay time information which is **specific to** an input terminal logical **state transition** and a resulting logical **state transition** at an output terminal, as required by claim 1.

For example, in the cited portions of Hasegawa '511 (e.g., at FIG. 3), a signal waveform for parts of the logic circuit 240 shown in FIG. 2 is shown. Specifically, FIG. 3 shows a timing

diagram for two inputs and an output of an OR gate (col. 4, lines 43-45; col. 1, lines 28 -35). However, there is no delay time information in Hasegawa '511 which is **specific to** an input terminal logical **state transition** (e.g., at input terminals 's' or 'v', see FIGS. 4 and 5) and a resulting logical **state transition** at an output terminal (e.g.,, at output terminal 't'). That is, the nullified states shown in Hasegawa '511, where no further action is required, are explicitly identified with respect to the state transitions at the input terminals and output terminal of the OR gate.

The delay times shown in FIGS. 12 and 13 are identified between the input terminals 's' or 'v' and the output terminal 't'. On the other hand, with the configuration set forth in claim 1, a target point at which no further delay analysis is required is automatically determined. For example, claim 1 recites that the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in said delay analysis library.

The above-noted distinctions were highlighted in the Amendment filed February 15, 2008. In response, in the Office Action mailed July 9, 2009 ("July 9th Office Action"), the Examiner contends that "**Hasegawa** '511 shows at Fig. 3 the logical state transitions at each input terminal and logical state transitions at each output terminal. **Hasegawa** '511 discusses at CL1, L28-35 the logical state transitions at the input terminal and the output terminal, using rise/fall terms. **Hasegawa** '511 states at CL2, L30-42 that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid). The logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **Hasegawa** '511 describes at CL3,

L5-26 that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified. Therefore, **Hasegawa** '511 teaches a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (CL2, L61-65)" (July 9th Office Action, page 17, first full paragraph). In the October 8th Amendment, Appellants respectfully disagreed as follows.

Appellants submitted that the invalidness specifier indicated by the invalidness specification in FIG. 7 of Hasegawa '511 is not, and cannot be, automatically generated unlike the delay time information of claim 1. This is because in Hasegawa '511, the "OR DEVICE" of FIG. 2 is not always an OR device, and moreover, there is no information provided in Hasegawa's alleged delay analysis library of what logical circuit is the subject of the delay analysis. Specifically, Hasegawa '511's FIG. 3 is merely one example, which does not form the basis that the information of FIG. 7 is correct in all cases. Thus, **manual** judgment is necessary for preparing the information indicated by the invalidness specifier of FIG. 7. On the other hand, in the present invention as claimed, the delay analysis library already comprises logical operation information which in turn comprises the delay information of the logical circuit, based on which the delay analyzing module can automatically analyze the delay of the logical circuit (e.g., the delay analyzing module, based on the delay time information, can generate indicative information that an action is invalid or valid). Hasegawa '511, alone, or in combination with Hasegawa '168, does not teach or suggest this feature.

The Examiner's response in the Final Office Action to these previously submitted arguments from the October 8th Amendment is basically the same as the July 9th Office Action (e.g., see Final Office Action, page 18, last paragraph, and July 9th Office Action, page 17, first full paragraph). The only difference in the Final Office Action is lines 2-7 on page 19, but here, the Examiner again points to previously cited portions of the references which allegedly teach that manual judgment is not necessary in Hasegawa '511 for preparing the information indicated by the invalidness specifier of FIG. 7. Appellants respectfully disagree.

For example, in the Examiner's response on page 19 of the Final Office Action, it is alleged that Hasegawa '168, in col. 1, lines 58-61 and col. 2, lines 30-35 teaches a library that already contains logical operation information. Appellants submit, however, that this logical operation does not teach or suggest all the features of the claimed logical operation information. For example, the claimed logical operation information comprises delay time information which is **specific to** an input terminal logical **state transition** and a resulting logical **state transition** at an output terminal. Although Hasegawa '168 discloses storing a delay time from each pin of a starting point in the logical circuit to a pin corresponding to the ending point, it does not teach or suggest that the stored delay time is specific to a state transition of the pin. Moreover, neither Hasegawa '511 nor Hasegawa '168 teach that the type of logic circuit which is the subject of delay analysis is prestored. As such, the delay analysis cannot be automatic, as required by claim 1. Consequently, Hasegawa '511 alone, or in combination with Hasegawa '168, does not render claim 1 obvious.

Claims 2-4 recite features similar to those discussed above with respect to claim 1. Therefore, claims 2-4 are patentable for *at least* reasons similar to those given above with respect to claim 1.

Conclusion

In view of the foregoing, Appellants respectfully request the Board to reverse the improper 35 U.S.C. § 112 and 35 U.S.C. § 103 rejections.

The USPTO is directed and authorized to charge the statutory fee (37 C.F.R. §41.37(a) and 1.17(c)) and all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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Date: August 24, 2009

CLAIMS APPENDIX

CLAIMS 1-6 ON APPEAL:

1. A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said delay analysis system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library,

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information comprising delay time information for a signal path from input terminals to output terminals of a logical circuit of said at least one circuit, wherein the delay time information is specific to an input terminal logical state transition of the logical circuit and resulting logical state transition at an output terminal of the logical circuit, and wherein said delay time information for each signal path of the logical circuit of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to the logical operation information,

wherein the delay analyzing module automatically analyzes the delay of the logical circuit based on the delay time information in said delay analysis library.

2. A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library,

wherein, for each of said plurality of circuits, said library further comprises respective logical operation information comprising respective delay time information for a signal path from input terminals to output terminals of a respective logical circuit of each of said plurality of circuits, wherein the respective delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for the respective logical circuit of each of said plurality of circuits, and wherein said delay time information for each signal path of said plurality of circuits is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to the respective logical operation information for each of said plurality of circuits,

wherein the delay analyzing module automatically analyzes the delay of the respective logical circuit of each of said plurality of circuits based on the respective delay time information in said delay analysis library.

3. A computer-implemented method of making a delay analysis of a logic circuit, comprising:

referencing, using a computer, a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information for said plurality of the circuits, wherein the delay

time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, said delay time information for each signal path of said logical circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for said at least one circuit; and

automatically selecting a delay time of each path of said logical circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information.

4. A computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

referencing a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic

operation information for said plurality of the circuits, wherein the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, said delay time information for each signal path of said logical circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for said at least one circuit;

automatically selecting a delay time of each path of said logical circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information; and

performing a delay calculation to determine a propagation delay time of the at least one circuit using said selected delay time of said logical circuit.

5. The delay analysis system as set forth in claim 1, wherein the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no

change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed.

6. The delay analysis system as set forth in claim 5, wherein the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case.

EVIDENCE APPENDIX:

No evidence is submitted herewith pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 and no other evidence has been entered by the Examiner and relied upon by Appellant in the appeal.

RELATED PROCEEDINGS APPENDIX

No decisions have been identified in Section II. Accordingly, no decisions are submitted herewith pursuant to 37 C.F.R. § 41.37(c)(1)(ii).